High performance printed organic transistors using a novel scanned thermal annealing technology

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Abstract

Printed organic thin film transistors (OTFTs) are a key component for the realization of low-cost, flexible electronics applications such as printed RFID tags or flexible displays. In recent years, great advances have been made in developing higher performance organic semiconductors. Many of these new materials show strongly process-dependent performance characteristics. The development of novel processing techniques is thus a key step towards utilizing the full potential of these semiconductor materials. Here we demonstrate a novel directional crystallization technique using a scanned thermal gradient to significantly improve the performance of printed OTFTs. A heat source is translated relative to the sample to induce the crystallization of the semiconductor. This scanned annealing creates a moving thermal gradient and thus develops a moving solvent evaporation gradient. Compared with uniform annealing on a hotplate grain size increases markedly and shows a clear directionality due to the separation of grain nucleation and growth. With this technique, mobility is boosted by about one order of magnitude. Mobilities close to $2cm^2/V\text{-}s$ can be achieved. Off-state performance is likewise improved as evidenced by a 3x improvement in subthreshold swing.

Keywords: Printed organic thin film transistors (OTFTs), directional crystallization, scanned thermal annealing, thermal gradient, mobility enhancement

1 Introduction

Printed organic electronics has been suggested as an enabling technology for a variety of novel applications such as printed RFID tags,[1,2] flexible displays[3], low-cost sensor networks[4,5] and smart packaging on paper.[6,7] One of the key devices for any such system are printed transistors. Performance of organic thin film transistors (OTFTs) has been improved significantly in recent years.[8–12] This includes improvements in both printing technology[13,14] and semiconductor materials.[15–17] However, many of these materials show strongly process dependent characteristics; as a result, while high performance devices have been demonstrated on idealized silicon-based test structures, performance has generally lagged in real printed devices on plastic. In particular, the semiconductor morphology in printed devices is generally much poorer than that achieved on smooth silicon substrates, resulting in degraded performance. Here we demonstrate a novel scanned thermal annealing technology that can be applied to plastic substrates to facilitate significant performance improvements. We employ a state of the art commercial organic semiconductor that has been shown to hold great promise for printed organic devices and circuits.[18–20] Similar acene based organic semiconductors have been studied extensively by John Anthony and co-workers.[21–23] Here we show that the directional crystallization resulting from scanned annealing of this solution processed, printable organic semiconductor can be exploited to significantly improve the performance of printed OTFTs , and demonstrate that high performance can indeed be achieved in printed devices on plastic substrates.

Directional crystallization techniques have been shown to significantly enhance the performance of inorganic semiconductors. Amorphous silicon can be crystallized into polysilicon by selective laser heating.[24–28] The crystallization mechanism involves melting and crystallization on solidification. By scanning the laser heat source, very large grains can be grown. This mechanism cannot be applied directly to solution processed semiconductors where the crystallization mechanism relies on the solvent being driven out of the film. This cannot be done repeatedly unlike melting and solidification of silicon, although there have been some reports for thick organic semiconductor films.[29,30] Multiple techniques have been reported to achieve directional crystallization of solution processed organic semiconductors. However, many of these techniques such as off-center spin coating[17] and crystallization on a tilted substrate[31] are incompatible with roll-to-roll fabrication and have not been shown to work well in realistic flexible substrates. Others, such as solution shearing[32,33] and zone casting[34–39] have shown great promise to leverage directional crystallization for improved electrical performance. However, most reports on solution sheared or zone cast films operate at very low speeds on the order of tens of micrometers per second. Our method operates at 1mm/second, which still requires further improvement, but is orders of magnitude faster than previous reports. A stationary thermal gradient has been used to enhance the performance of solution processed TIPS-pentacene transistors.[40] This work demonstrates the benefit of thermal gradients for the crystallization of solution processed organic semiconductors, however, does not allow sufficient control due to inherent temperature variations across the sample, particularly when using flexible substrates and printed electronics processes.

Here we demonstrate a novel technique, which utilizes a scanned thermal gradient to induce the directional crystallization of a solution processed organic semiconductor. A plastic substrate is translated relative to a heated metal bar that is in contact with the bottom side of the plastic substrate (**see Figure 1 (a)** for an illustration of the technique); since the scanning process inherently exploits the relative motion of the substrate, it is very compatible with roll-to-roll processing. The top side contains devices with the solution deposited semiconductor. A thermal gradient is induced within the plastic substrate at the edge of the heated bar. This leads to a gradient in solvent evaporation rate and thus a gradient in the crystallization driving force. This gradient is scanned across the substrate as the heated bar is translated. The effect of this technique on crystallization is illustrated in **Figure 2 (a)**. To understand this, it

behooves us to first summarize the kinetics of crystallization. Crystallization is typically described by two phenomena, nucleation and grain growth. Nucleation describes the process by which initial crystallites are formed, while grain growth describes the process by which these crystallites enlarge. Typically, the activation energy for nucleation exceeds that of grain growth; as a consequence, once grains nucleate, they typically grow to fill the available space between nuclei. As a consequence, grain size is typically limited by the density of initial nuclei. Uniform heating as conventionally used leads to the uniform nucleation of grains, which will then grow essentially isotropically. The final grain size is thus determined by the initial nucleation density. By using a scanned heating source, a gradient in crystallization driving force can be introduced using our novel technique, enhancing grain growth in preferred orientations relatively to nucleation. After some initial nucleation, grains can grow freely without impinging on further grains since no grains have nucleated ahead of the gradient yet. This will lead to significantly enlarged grains that are elongated and aligned with the scanning direction. The details of the crystallization process will also depend on interactions with the source and drain electrodes as illustrated in Figure 2 (b). This will be discussed in more detail below.

2 Materials and methods

2.1 Materials

Devices were fabricated on planarized polyethylene naphthalate (PEN) substrates provided by DuPont Teijin Films. The gate, source and drain electrodes were fabricated using CCI-300, a silver nanoparticle ink purchased from Cabot Corporation. 2-Heptanone purchased from Sigma Aldrich was used to dilute the gate dielectric ink. All other materials were purchased from EMD Chemicals: lisicon® D207 (gate dielectric polymer ink, diluted with 2-Heptanone), lisicon® M001 (surface treatment for the source and drain electrodes, used as received) and lisicon® S1200 (small molecule acene based organic semiconductor dissolved in Mesitylene (boiling point 165°C) and Cyclohexylbenzene (boiling point 240°C), used as received).

2.2 Fabrication processes, characterization and simulation

Bottom-gate bottom-contact transistors were fabricated to study the crystallization mechanism and electrical performance characteristics of the scanned thermal annealing technique demonstrated here. (see Figure 1 (b) for device structure). PEN substrates were laser cut to a size of 9cm by 4cm of which an area of 4cm by 4cm was used for device fabrication. Silver gate electrodes were inkjet-printed using CCI-300 followed by sintering at 150°C for 30 minutes. The polymer gate dielectric lisicon® D207 was deposited by spin coating at 3000RPM. The ink as received was diluted 1:1 by volume with 2-Heptanone before spin coating. This resulted in an average film thickness of 330nm. The spun layer was UV cross-linked for 10 minutes (λ=365nm, 3J/cm^2). After a short UV ozone treatment for 2 minutes the source and drain electrodes were deposited by inkjet printing. The same CCI-300 ink and sintering conditions were used as for the gate electrode. Before depositing the semiconductor a two-step surface treatment was applied. The source and drain electrodes and the channel region were exposed to a forming gas RF plasma for 30 seconds at 40W. Within 5 minutes after the plasma cleaning step lisicon® M001 was applied by drop casting. After spin drying, the samples were rinsed with isopropyl alcohol and spin dried again. The semiconductor lisicon® S1200 was applied by spin coating. A high spin speed of 9000 RPM was chosen to realize thin semiconductor layers, minimizing short channel effects. The

semiconductor was crystallized by uniform and by scanned annealing. Both were performed at the same temperature 100°C. Uniform annealing was done on a standard hotplate for 1 minute. A custom built set-up was used for scanned annealing (see Figure 1 (a) for an illustration). The PEN substrate with devices on top was pushed onto a heated aluminum bar. The bar was heated by a fire rod inserted into the bar and the temperature was controlled by a thermocouple attached to the bar close to the area used for annealing. The bar was then scanned at a speed of 1mm/s relative to the substrate. Both uniformly annealed devices and devices with scanned annealing were subjected to a 5 minute post-anneal at 100°C on a hotplate to reduce the defect density and improve performance. Transistor characteristics were measured using an Agilent 4156C semiconductor parameter analyzer in a nitrogen atmosphere. All fabrication steps were performed in air.

The temperature distribution and heat flow inside the plastic substrate were studied by numerical simulations using COMSOL Multiphysics.

3 Simulation of thermal gradient

The key to achieving a reliable, sharp thermal gradient is the correct choice of substrate. The substrate needs to fulfill three criteria. Firstly, since heat is conducted through the thickness of the substrate, a thin substrate is desirable. This guarantees fast heat conduction to the top surface. Secondly, heat must not spread too quickly laterally along the substrate. Otherwise the thermal gradient is rapidly washed out and the temperature profile approaches the condition of uniform heating. Therefore the thermal conductivity of the substrate must be limited. Thirdly, heat is coupled into the substrate through a mechanical contact with the heated bar. This is enhanced through a conformal contact, which requires the substrate to be flexible. All three requirements suggest that plastic is an ideal substrate for this application. This was verified by numerical simulations solving the heat diffusion equation:

$$\rho c_p \frac{\partial T}{\partial t} - \nabla(k \nabla T) = 0 \qquad (1)$$

The substrate material parameters that determine the result of this equation are ρ the material's density, c_p the material's specific heat capacity and k the material's thermal conductivity. The numerical values of these parameters as used in our simulations are listed in **Table 1**. The heat diffusion equation was solved to determine temperature T as a function of time t and position. The boundary conditions for the bottom surface of the substrate simulate the moving heated bar. A constant hot temperature is assumed for the heated region. The unheated region is assumed to be thermally isolated. The boundary between the two regions is moved with time. This boundary condition corresponds to a moving step function in external temperature. In reality the moving bar corresponds to a moving pulse, however, since the width of the bar is much larger than the width of the thermal gradient in the plastic substrate (1cm vs. about 500µm), this is an accurate boundary condition to simulate the thermal gradient at the leading edge of the real bar. The boundary conditions for the other surfaces on the side and top of the plastic substrate are set to be natural convection. **Figure 3 (a)** shows a typical simulation result at one time point for PEN (polyethylene naphthalate), a common plastic substrate for printed electronics. This result shows that a sharp thermal gradient develops throughout the PEN film. In order to compare the evolution of this thermal gradient with time and compare PEN with silicon, the thermal profile along the top surface of the substrate was recorded for different points in time. These multiple temperature profiles for different times were plotted on the same axes (see Figure 3 (b)). The thermal gradient on top of PEN is sharp and steady and only shifted in position as time progresses despite of the fact

that the heater is dynamically translated. Conversely, silicon does not exhibit a steady thermal gradient. The gradient very quickly diminishes as heat spreads uncontrollably fast laterally through the substrate. This shows that plastic substrates exhibit beneficial thermal properties for directional crystallization utilizing a scanned thermal gradient. This is a very important finding for flexible electronics applications.

4 Results and discussion

4.1 Device performance

Devices fabricated using scanned thermal annealing exhibit significantly improved electrical performance when compared with devices fabricated using uniform annealing. Representative transfer characteristics for short channel devices can be observed in **Figure 4 (a)**. Median transistor parameters are summarized in **Table 2**. The greatest improvements can be observed for short channel devices where the thermal gradient is scanned in parallel with the electrodes. Mobility is increased by an order of magnitude from around 0.1cm^2/V-s to over 1cm^2/V-s. Off-state characteristics are also improved in terms of subthreshold swing and turn-on voltage. On-off ratio is good in all cases. This significant improvement is due to a greatly enhanced grain size. One can clearly observe the difference between uniformly annealed samples, which exhibit randomly oriented grains, and samples annealed by the scanned thermal gradient, which exhibit elongated grains of much larger size (see **Figure 5**Figure 6). Grains are aligned with the scanning direction providing evidence of a successful separation of nucleation and growth during crystallization. This is not only observed in areas away from devices but also in the channel region of transistors (see **Figure 6**). This observation is especially clear for long channel devices.

In order to understand the crystallization mechanism better and to optimize performance, devices with different channel lengths and scanning directions were fabricated. Two different scanning directions were investigated: in parallel and perpendicular to the gate and source/drain electrodes (see Figure 6 for illustration). A Welch's t-test was performed on the experimentally obtained saturation mobility distributions to identify statistically significant differences between conditions. Statistically significant differences were found between uniformly annealed devices and devices with scanned annealing in both directions. Significant differences were also found between the two different scanning directions for long channel devices. Short and long channel devices were also found to exhibit significantly different performance in the cases of both uniform annealing and scanning parallel to the electrodes. However, for short channel devices no statistically significant differences were found between the scanning directions. For scanning perpendicular to the electrodes, no statistically significant differences were found between short and long channel devices either. These effects can be explained by considering both crystallization effects and the effect of contact resistance.

4.2 Effect of channel length

Both uniformly annealed devices and devices with scanned annealing parallel to the electrodes exhibit increased performance for longer channels compared with shorter channel devices annealed under the same conditions. One reason is the preferred nucleation of the semiconductor on the electrodes. This leads to smaller grains on and close to the electrodes. This disruption of the crystallization will impact short channel devices more severely because the region close to the electrodes makes up a larger portion of the channel. Secondly, short channel devices are limited by contact resistance due to a contact barrier. This has been

minimized with a surface treatment, however, has not been eliminated completely. In the case of short channel devices the mean saturation mobility is about 30% higher than the mean linear mobility due to the larger effect of contact resistance in the linear regime. For long channel devices this difference is reduced to about 10% as one would expect due to the larger influence of channel resistance compared with contact resistance. Both effects combined lead to the limited performance of short channel devices.

4.3 Effect of scanning direction

Devices fabricated using scanning perpendicular to the electrodes generally exhibit lower performance than devices fabricated by scanning parallel to the electrodes. The worst case devices and the variability of performance tend to be worse for devices fabricated using scanning perpendicular to the electrodes (see Figure 4 (b) for boxplot of saturation mobility). The difference in mean saturation mobility between scanning directions is more pronounced and only statistically significant for long channel devices. Long channel devices fabricated by perpendicular scanning are limited in performance despite the smaller effect of contact resistance compared with shorter channel devices. Therefore no significant effect of channel length can be observed for perpendicular scanning. To understand this effect, we may consider the details of the crystallization mechanism. This is schematically illustrated in Figure 2 (b). For perpendicular scanning the thermal gradient will initially approach one of the source/ drain electrodes (the upper electrode in Figure 6). Nucleation will occur on this electrode and then grains will grow into the channel without further nucleation, leading to elongated grains. As the thermal gradient approaches the second (bottom) electrode, further nucleation will occur on this electrode. These secondary grains can grow back into the channel impinging on the elongated primary grains growing from the primary (top) electrode. This creates significant disorder and smaller grains close to the second electrode, which will limit device performance, and can be observed clearly for the long channel devices in Figure 6 (d) and (e) and is illustrated in Figure 2 (b). This mechanism does not exist for devices fabricated using scanning parallel to the electrodes. In these devices, grains grow from both electrodes simultaneously and only impinge once at the center of the channel (see both Figure 2 (b) and Figure 6 (h)). This explains the improved performance of devices where the thermal gradient is scanned in parallel with the electrodes. Further, in the case of devices fabricated using scanning perpendicular to the electrodes, short channel devices are less limited by primary grains impinging on secondary grains since both primary and secondary grains can bridge shorter channels more easily as the size of the secondary grains is comparable to the channel length. This effect is offset by the effect of contact resistance. Considering these effects together, both the crystallization and contact resistance effects then result in no net difference in performance between short and long channel devices when the thermal gradient is scanned perpendicular to the electrodes. However, even with this slightly lessened improvement in devices fabricated by scanning perpendicular to the electrodes, the scanning technique clearly gives significant improvement in performance across all device geometries relative to uniform annealing. Indeed, scanning perpendicular to the channel results in devices with more uniform device characteristics across all channel lengths, which is beneficial for the design of realistic circuits. The significant performance improvement across the board under these conditions is very attractive, as a result.

5 Conclusion

Future work using X-ray scattering and/or polarized spectroscopy measurements could be undertaken to further understand the origins of the significant performance improvements we

observe. Such measurements would have to account for the contacts, which clearly strongly affect crystallization.

To conclude, a novel crystallization technique was demonstrated utilizing a scanned thermal gradient to anneal a solution processed, printable organic semiconductor. This leads to significantly improved electrical performance as well as significantly enlarged grains. Optimum crystallization and electrical performance can be obtained when scanning in parallel with the source and drain electrodes. The process is inherently compatible with roll-to-roll processing and flexible substrates, and results in significant performance improvements in printed organic transistors.

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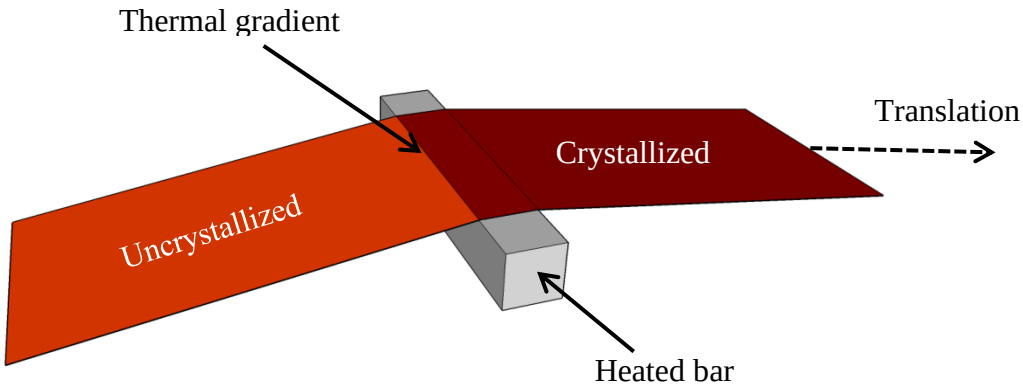
[1] V. Subramanian, J. M. J. Frechet, P. C. Chang, D. C. Huang, J. B. Lee, S. E. Molesa, A. R. Murphy, D. R. Redinger, S. K. Volkman, *Proc. IEEE* **2005**, *93*, 1330.
[2] Namsoo Lim, Jaeyoung Kim, Soojin Lee, Namyoung Kim, Gyoujin Cho, *Adv. Packag. IEEE Trans. On* **2009**, *32*, 72.
[3] T. Sekitani, H. Nakajima, H. Maeda, T. Fukushima, T. Aida, K. Hata, T. Someya, *Nat Mater* **2009**, *8*, 494.
[4] J. B. Chang, V. Liu, V. Subramanian, K. Sivula, C. Luscombe, A. Murphy, J. Liu, J. M. J. Fréchet, *J. Appl. Phys.* **2006**, *100*, 014506.
[5] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, *Proc. Natl. Acad. Sci. U. S. A.* **2005**, *102*, 12321.
[6] D. Tobjörk, R. Österbacka, *Adv. Mater.* **2011**, *23*, 1935.
[7] G. Grau, R. Kitsomboonloha, S. L. Swisher, H. Kang, V. Subramanian, *Adv. Funct. Mater.* **2014**.
[8] Y.-Y. Noh, N. Zhao, M. Caironi, H. Sirringhaus, *Nat Nano* **2007**, *2*, 784.
[9] H.-Y. Tseng, V. Subramanian, *Org. Electron.* **2011**, *12*, 249.
[10] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, V. Subramanian, *Org. Electron.* **2010**, *11*, 2037.
[11] H. Kang, R. Kitsomboonloha, J. Jang, V. Subramanian, *Adv. Mater.* **2012**, *24*, 3065.
[12] A. Pierre, M. Sadeghi, M. M. Payne, A. Facchetti, J. E. Anthony, A. C. Arias, *Adv. Mater.* **2014**, n/a.
[13] R. Kitsomboonloha, S. J. S. Morris, X. Rong, V. Subramanian, *Langmuir* **2012**, *28*, 16711.
[14] R. Kitsomboonloha, V. Subramanian, *Langmuir* **2014**, *30*, 3612.
[15] I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner, W. Zhang, M. L. Chabinyc, R. J. Kline, M. D. McGehee, M. F. Toney, *Nat. Mater.* **2006**, *5*, 328.
[16] J. Smith, R. Hamilton, I. McCulloch, N. Stingelin-Stutzmann, M. Heeney, D. D. C. Bradley, T. D. Anthopoulos, *J. Mater. Chem.* **2010**, *20*, 2562.
[17] Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. B. Mannsfeld, J. Chen, D. Nordlund, M. F. Toney, J. Huang, Z. Bao, *Nat. Commun.* **2014**, *5*, DOI 10.1038/ncomms4005.
[18] K. Fukuda, Y. Takeda, Y. Yoshimura, R. Shiwaku, L. T. Tran, T. Sekine, M. Mizukami, D. Kumaki, S. Tokito, *Nat. Commun.* **2014**, *5*, DOI 10.1038/ncomms5147.
[19] K. Fukuda, Y. Takeda, M. Mizukami, D. Kumaki, S. Tokito, *Sci. Rep.* **2014**, *4*, DOI 10.1038/srep03947.
[20] Y. Yoshimura, Y. Takeda, K. Fukuda, D. Kumaki, S. Tokito, *Org. Electron.* **2014**, *15*, 2696.
[21] J. E. Anthony, D. L. Eaton, S. R. Parkin, *Org. Lett.* **2002**, *4*, 15.
[22] S. K. Park, T. N. Jackson, J. E. Anthony, D. A. Mourey, *Appl. Phys. Lett.* **2007**, *91*, 063514.
[23] R. Hamilton, J. Smith, S. Ogier, M. Heeney, J. E. Anthony, I. McCulloch, J. Veres, D. D. C. Bradley, T. D. Anthopoulos, *Adv. Mater.* **2009**, *21*, 1166.
[24] M. Hatano, S. Moon, M. Lee, K. Suzuki, C. P. Grigoropoulos, *J. Appl. Phys.* **2000**, *87*, 36.
[25] M. Lee, S. Moon, C. P. Grigoropoulos, *J. Cryst. Growth* **2001**, *226*, 8.
[26] S.-G. Ryu, I. Gruber, C. P. Grigoropoulos, D. Poulikakos, S.-J. Moon, *Thin Solid Films* **2012**, *520*, 6724.
[27] M. Lee, S. Moon, M. Hatano, K. Suzuki, C. P. Grigoropoulos, *J. Appl. Phys.* **2000**, *88*, 4994.
[28] R. S. Sposili, J. S. Im, *Appl. Phys. Lett.* **1996**, *69*, 2864.
[29] C.-Y. Liu, A. J. Bard, *Chem. Mater.* **2000**, *12*, 2353.

[30] G. Schweicher, N. Paquay, C. Amato, R. Resel, M. Koini, S. Talvy, V. Lemaur, J. Cornil, Y. Geerts, G. Gbabode, *Cryst. Growth Des.* **2011**, *11*, 3663.
[31] Y. Natsume, T. Minakata, T. Aoyagi, *Org. Electron.* **2009**, *10*, 107.
[32] H. A. Becerril, M. E. Roberts, Z. Liu, J. Locklin, Z. Bao, *Adv. Mater.* **2008**, *20*, 2588.
[33] J. Soeda, T. Uemura, T. Okamoto, C. Mitsui, M. Yamagishi, J. Takeya, *Appl. Phys. Express* **2013**, *6*, 076503.
[34] A. Tracz, J. K. Jeszka, M. D. Watson, W. Pisula, K. Müllen, T. Pakula, *J. Am. Chem. Soc.* **2003**, *125*, 1682.
[35] W. Pisula, A. Menon, M. Stepputat, I. Lieberwirth, U. Kolb, A. Tracz, H. Sirringhaus, T. Pakula, K. M**?**llen, *Adv. Mater.* **2005**, *17*, 684.
[36] P. Miskiewicz, M. Mas-Torrent, J. Jung, S. Kotarba, I. Glowacki, E. Gomar-Nadal, D. B. Amabilino, J. Veciana, B. Krause, D. Carbone, C. Rovira, J. Ulanski, *Chem. Mater.* **2006**, *18*, 4724.
[37] C. M. Duffy, J. W. Andreasen, D. W. Breiby, M. M. Nielsen, M. Ando, T. Minakata, H. Sirringhaus, *Chem. Mater.* **2008**, *20*, 7252.
[38] P. Miskiewicz, S. Kotarba, J. Jung, T. Marszalek, M. Mas-Torrent, E. Gomar-Nadal, D. B. Amabilino, C. Rovira, J. Veciana, W. Maniukiewicz, J. Ulanski, *J. Appl. Phys.* **2008**, *104*, 054509.
[39] I. Tszydel, M. Kucinska, T. Marszalek, R. Rybakiewicz, A. Nosal, J. Jung, M. Gazicki-Lipman, C. Pitsalidis, C. Gravalidis, S. Logothetidis, M. Zagorska, J. Ulanski, *Adv. Funct. Mater.* **2012**, *22*, 3840.
[40] C.-M. Keum, J.-H. Kwon, S.-D. Lee, J.-H. Bae, *Solid-State Electron.* **2013**, *89*, 189.

(a)



(b)

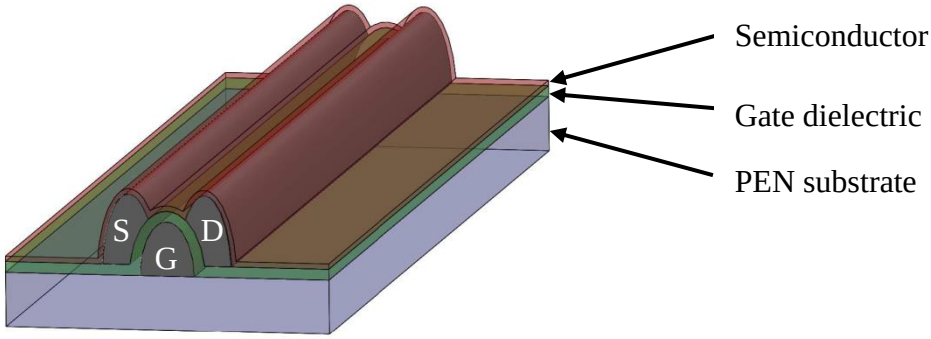
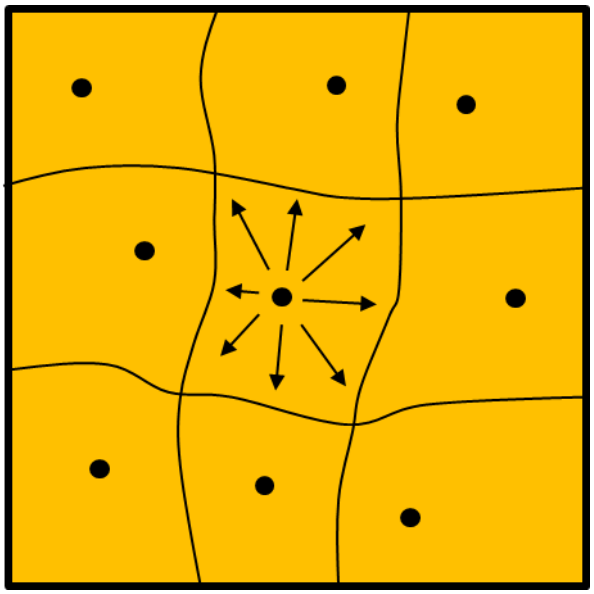


Figure 1 (a) Scanned thermal annealing method. A plastic substrate is brought in contact with a heated metal bar and translated to the right relative to the bar. OTFTs with the organic semiconductor are located on top of the plastic substrate. A thermal gradient and thus solvent evaporation gradient exists inside the plastic substrate at the leading edge of the heated bar. Crystallization occurs at the location of the gradient. The semiconductor material to the left of the thermal gradient has not crystallized yet whereas material to the right of it has already crystallized. (b) Device structure of printed OTFTs.

(a)
(i)



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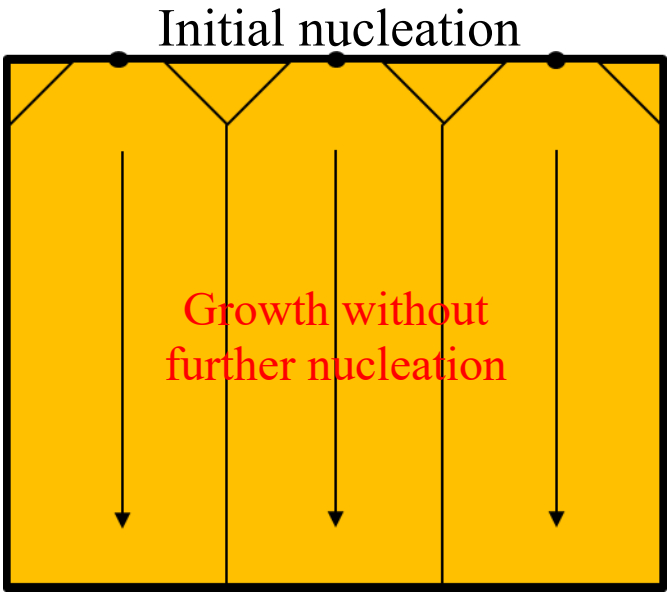

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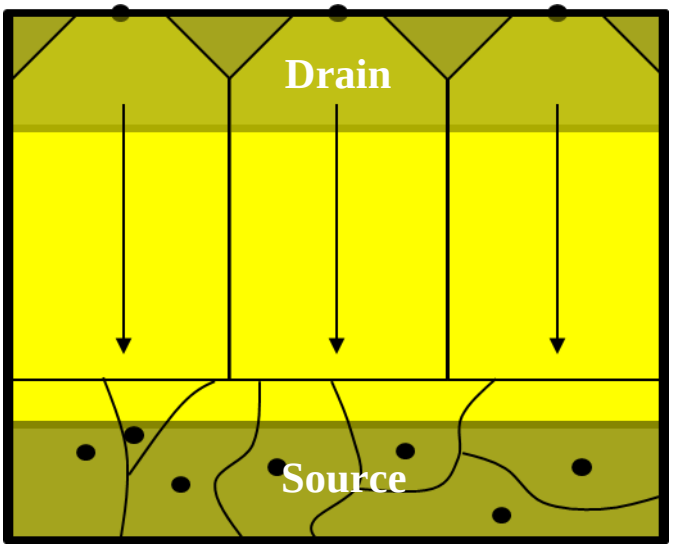

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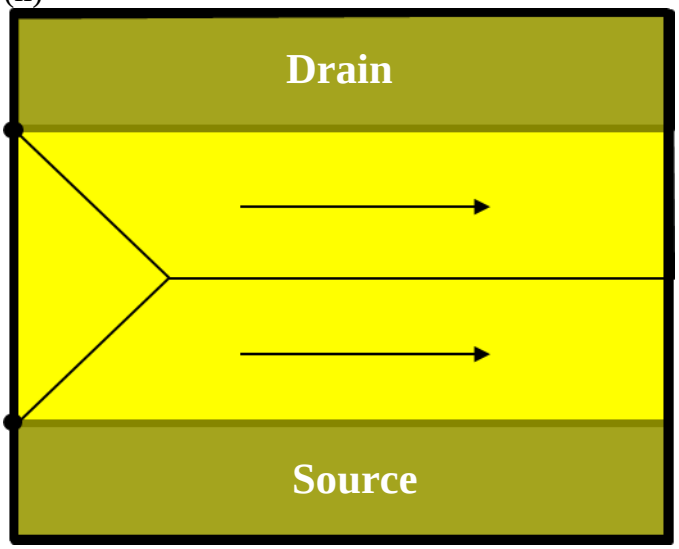

Figure 2. (a) Illustration of the crystallization mechanism for (i) uniform and (ii) scanned annealing. Uniform heating leads to uniform nucleation and growth. Scanned thermal annealing leads to a separation of nucleation and growth and thus significantly enlarged elongated grains. (b) Illustration of scanned thermal annealing crystallization mechanism including the source and drain electrodes for scanning (i) perpendicular to and (ii) in parallel with the electrodes. Preferred nucleation on the electrodes disrupts the crystallization. For scanning perpendicular to the electrodes this leads to small secondary grains close to the bottom electrode, which limits performance compared with parallel scanning where elongated grains do not impinge on secondary grains since grains grow in parallel with electrodes rather than towards one.

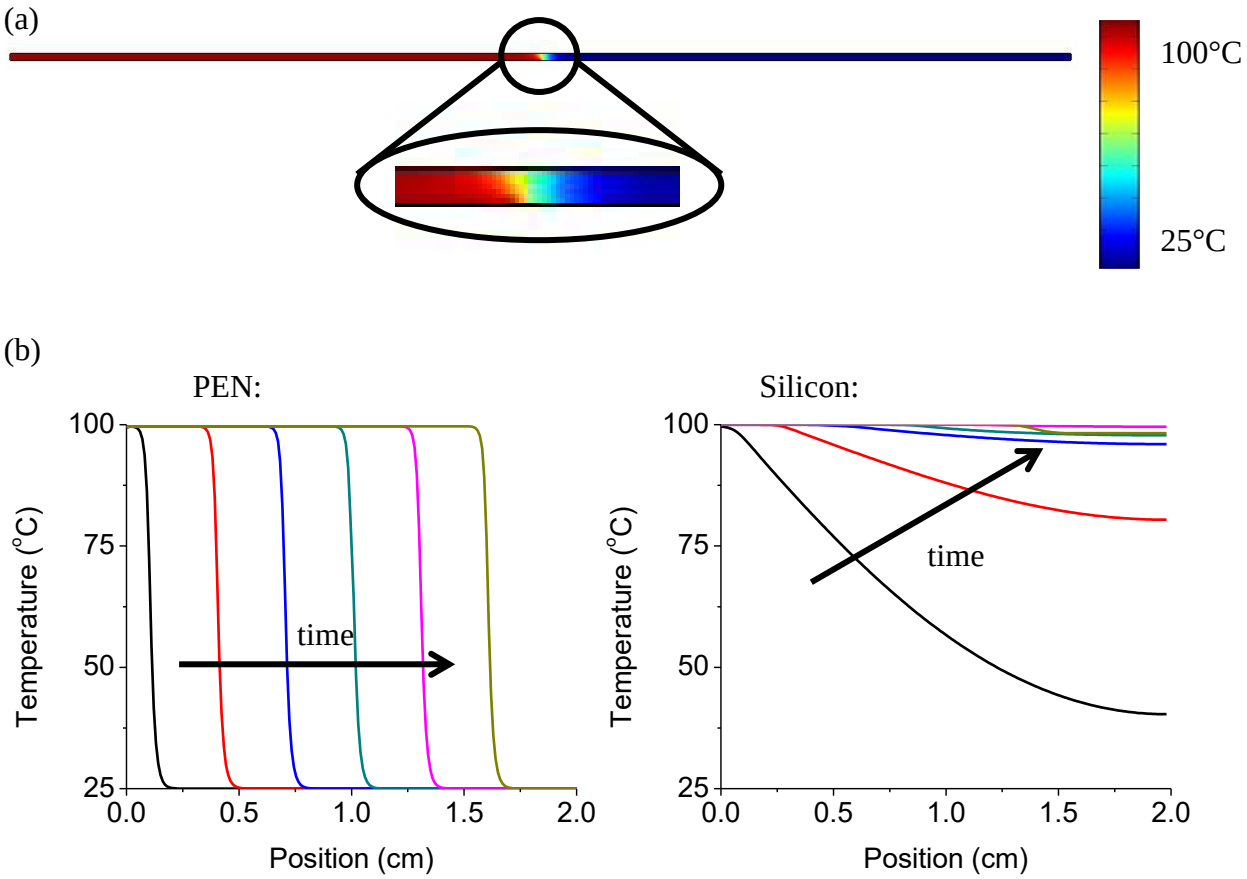

Figure 3. (a) Simulated temperature distribution within PEN substrate (side view with translating heater on the bottom left). This shows a clear separation between the hot zone on the left, heated by the metal bar, and the insulated cold zone on the right. The boundary between the two zones is translated to simulate the moving heater. This result is a snapshot in time as the thermal gradient is translated along the length of the PEN substrate. (b) Temperature distribution along the top surface of the PEN and silicon substrates. Each curve corresponds to a different point in time as the heater is translated. PEN shows a sharp thermal gradient that stays constant and only shifts in position as the heater is translated from left to right. The thermal gradient in silicon very quickly diminishes as heat spreads rapidly laterally.

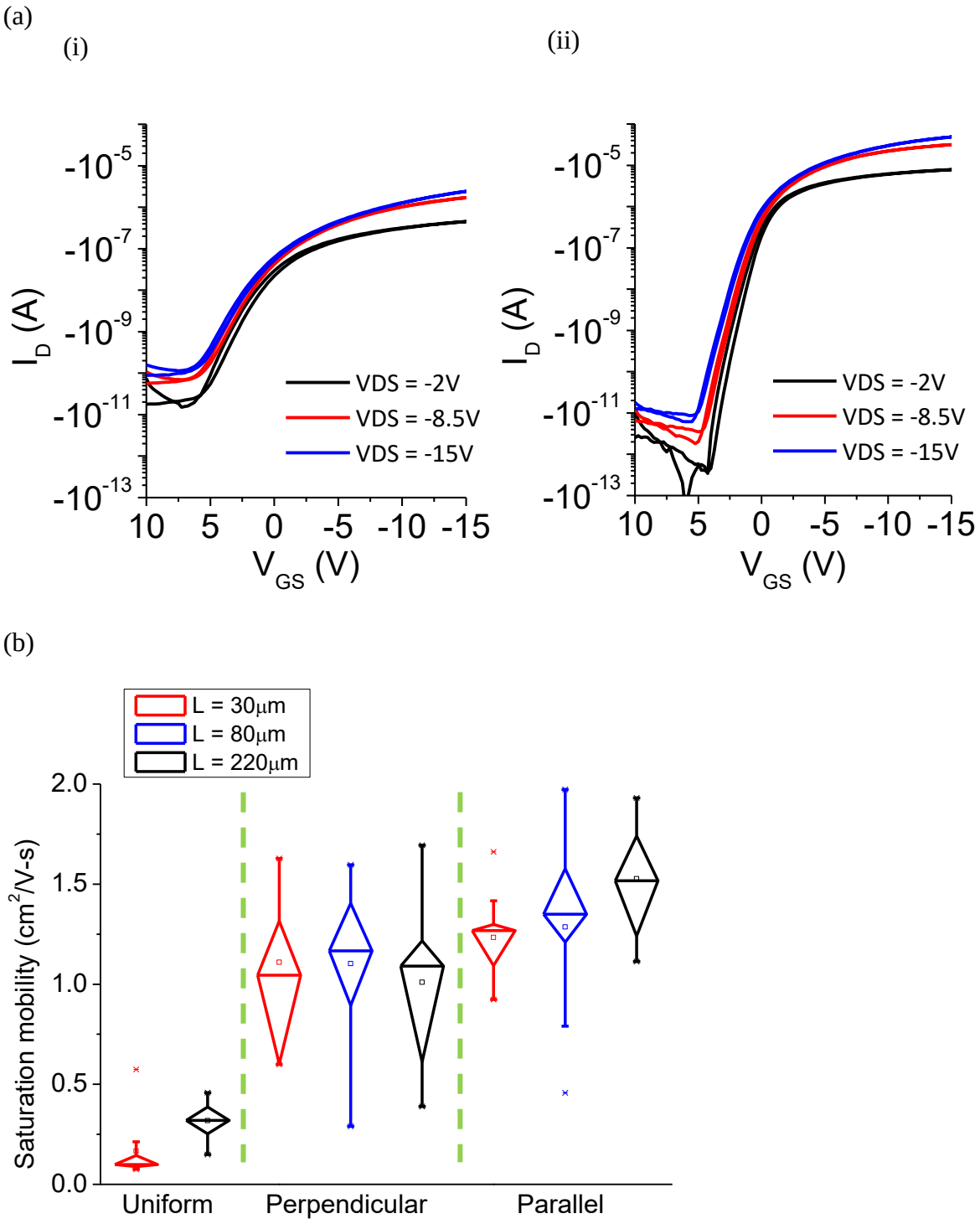

Figure 4. (a) Representative transfer characteristics of short channel devices (25μm channel length and 830μm channel width) crystallized by (i) uniform heating and (ii) scanned thermal anneal (scanning direction in parallel with electrodes). The switching performance is significantly improved by scanned annealing both in the on- and off-state. (b) Boxplot comparing performance statistics of different annealing conditions (uniform annealing, scanning perpendicular and scanned parallel to electrodes) and channel lengths.

(a)

(b)

50μm

Figure 5. Polarized optical microscope images showing crystallization away from transistors. (a) Uniform annealing. Randomly oriented small grains. (b) Scanned thermal annealing. Arrow indicates scanning direction. Grains are clearly enlarged and aligned with the scanning direction as expected for the successful separation of nucleation and growth.

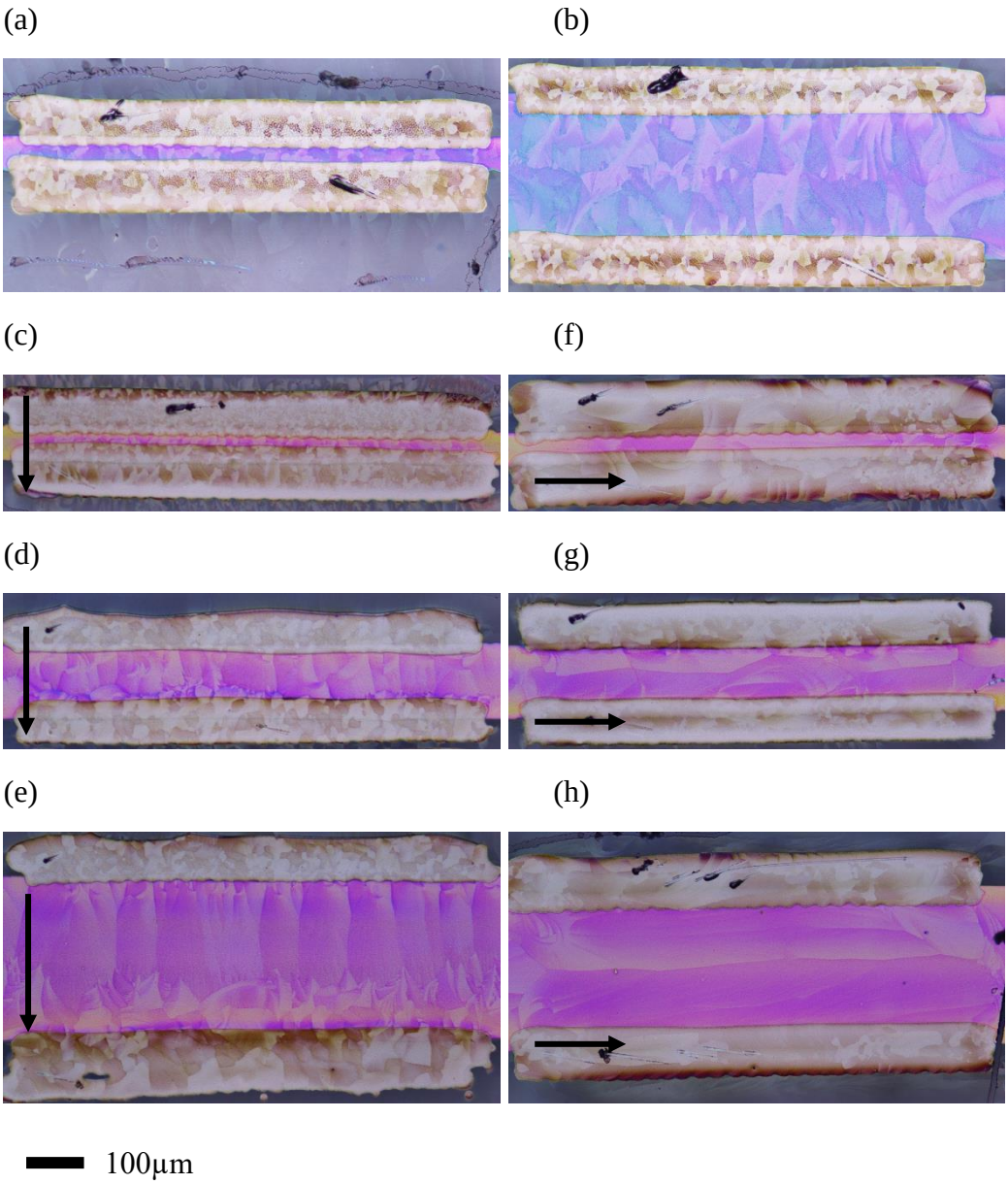

Figure 6. Polarized optical micrographs of grain structure for different annealing conditions. Black arrow indicates scanning directions. (a)&(b) Uniform annealing. Grains are randomly oriented and small. (c)-(e) Scanned thermal annealing perpendicular to electrodes. Grains are elongated and aligned with the scanning direction. Small secondary grains impinge on large primary grains close to the second electrode. This is most prevalent for long channel devices. (f)-(h) Scanned thermal annealing in parallel with electrodes. Grains are again aligned with the scanning direction and have the largest size of all the tested conditions. No impingement on secondary grains is observed.

Table 1. Material parameters used for simulation of thermal gradient

Parameter	Silicon	PEN
ρ (kg/m^3)	2329	1380
c_p (J/kg*K)	700	1000
k (W/m*K)	130	0.2

Table 2. Median values of transistor characteristics for different channel lengths and annealing methods

L [µm]	Anneal	Linear mobility [cm^2/V-s]	Saturation mobility [cm^2/V-s]	On-off ratio	Subthreshold swing [V/dec]	V_{on} [V]
30	Uniform	0.086	0.099	1.0*10^5	1.27	7.50
30	Scanned perpendicular	0.90	1.08	2.4*10^7	0.49	6.63
30	Scanned parallel	0.98	1.27	2.9*10^6	0.46	5.25
220	Uniform	0.26	0.32	1.8*10^4	1.77	7.00
220	Scanned perpendicular	0.91	1.09	2.0*10^4	0.55	0.50
220	Scanned parallel	1.34	1.52	1.1*10^6	0.52	2.00